PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: MARK B. FUSELIER DERICK J. WRISTERS ANDY C. WEI	Confirmation No.: 9406 Examiner: Donghee Kang
Serial No.: 10/821,230	Group Art Unit: 2811
Filed: April 8, 2004	Att'y Docket: 2000.092182/TT5077D
For: SEMICONDUCTOR DEVICE FORMED OVER A MULTIPLE THICKNESS BURIED OXIDE LAYER, AND METHODS OF MAKING SAME	Customer No.: 23720

APPEAL BRIEF

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences in response to the Final Office Action dated February 15, 2006. The Notice of Appeal was filed on April 12, 2006.

The Director is authorized to deduct the fee for filing this Appeal Brief ($500), or any additional fees under 37 C.F.R. §§ 1.16 to 1.21 required for any reason relating to this document, from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.092182.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Applicants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-30 and 56-64 are pending in the application. Claims 1-30 and 56-64 are at issue in this appeal and they are attached as Appendix A. Claims 1-30 and 56-64 were rejected in the Final Office Action issued on February 15, 2006. Claims 1-30 and 56-64 are the subject of the present appeal.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In general, the present invention is directed to semiconductor fabrication technology, and, more particularly, to a semiconductor device formed over a multiple thickness buried oxide layer. There are six independent claims at issue in the current appeal: claims 1, 13, 23, 56, 58 and 60.

Independent claim 1 is generally directed to a semiconductor device 10 including a bulk substrate 12, an active layer 21 and a multiple thickness buried oxide layer 20 (comprised of regions 20A and 20B) formed between the bulk substrate 12 and the active layer 21. The multiple thickness buried oxide layer 20 has a substantially planar upper surface that contacts the active layer 21 and a non-planar lower surface that contacts the bulk substrate 12. The active layer 12 is formed above the multiple thickness buried oxide layer 20, and the semiconductor device 10 is formed in the active layer 21 above the multiple thickness buried oxide layer 20. By

way of example only, at least portions of the invention are described at page 8, line 1 – page 9, line 18; Figure 1.

Independent claims 13 and 23 are similar to claim 1 but specifically recite more detail regarding the configuration of the multiple thickness buried oxide layer 20. As with claim 1, claim 13 recites that the buried oxide layer 20 comprises a substantially planar upper surface that contacts the active layer 21 and a non-planar lower surface that contacts the bulk substrate 21. Claim 13 also recites that the buried oxide layer 20 comprises a first section positioned between two second sections, wherein the first section has a thickness and each of the second sections have a thickness, and wherein the thickness of the first section is less than the thickness of the second sections.

Independent claim 56 is generally directed to a semiconductor device 10 including a bulk substrate 12, an active layer 21 and a multiple thickness buried oxide layer 20 formed between the bulk substrate 12 and the active layer 20. The multiple thickness buried oxide layer 20 comprises a substantially planar upper surface that contacts the active layer 21 and a non-planar lower surface that contacts the bulk substrate 12. The active layer 21 is formed above the multiple thickness buried oxide layer 20. The device 10 is formed in the active layer 21 above the multiple thickness buried oxide layer 20. Claim 56 further requires a doped back gate region 13 positioned at least partially in the bulk substrate 12 under the multiple thickness buried oxide layer 20. By way of example only, at least portions of the invention are described at page 8, line 1 – page 9, line 18; page 12, line 1 – page 13, line 4; Figure 4.

Independent claims 58 and 60 are similar to claim 56 but contain additional details regarding the precise structure of the buried oxide layer 20, similar to the limitations set forth above with respect to claims 13 and 23.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-5, 7-11, 13-16, 18-21, 23-25, 27-27 and 56-64 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Wu (U.S. Patent No. 6,441,436).

2. Claims 6, 17 and 26 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wu in view of Shigyo (U.S. Patent No. 5,760,442).

3. Claims 12, 22 and 30 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wu.

VII. ARGUMENT

A. Legal Standards

As the Board well knows, an anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). To the extent the Examiner relies on principles of inherency in making the anticipation rejections in the Office Action, inherency requires that the asserted proposition necessarily flow from the disclosure. *In re Oelrich*, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981); *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1463-64 (Bd. Pat. App. & Int. 1990); *Ex parte Skinner*, 2 U.S.P.Q.2d 1788, 1789 (Bd. Pat. App. & Int. 1987); *In re King*, 231 U.S.P.Q. 136, 138 (Fed. Cir. 1986). It is not enough that a reference could have, should have, or would have been used as the claimed invention. "The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Oelrich*, at 326, quoting *Hansgirg v. Kemmer*, 40 U.S.P.Q. 665, 667 (C.C.P.A. 1939); *In re Rijckaert*, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993), quoting *Oelrich*, at 326; see also *Skinner*, at 1789. "Inherency … may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a

given set of circumstances is not sufficient." *Skinner*, at 1789, citing *Oelrich*. Where anticipation is found through inherency, the Office's burden of establishing prima facie anticipation includes the burden of providing "...some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art." *Skinner* at 1789.

Moreover, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Health-care Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the

desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

B. <u>The Rejections and the Prior Art</u>

In making the rejections on appeal, the Examiner identified the bulk substrate in Wu as being the combination of items 103, 102 and 101b, and the layer 101a as the active layer. Final Office Action, p. 2. The combination of items 104 and 212a were asserted to be the "multiple thickness buried oxide layer." *Id*. The Examiner also identified the item 101b as a doped back gate region. Final Office Action, p. 3. Respectfully, the Examiner's reading and interpretation of Wu reflects fundamental error.

SOI structures are well known in the art. As indicated in the specification, the SOI structure depicted therein is comprised of a bulk substrate 12, a buried insulation layer 20 and an active layer 21. This description is consistent with the well-known structure of SOI substrates. It is respectfully submitted that, in rejecting the pending claims, the Examiner either confused or contorted the structures depicted in Wu to conclude that such an SOI substrate was disclosed in Wu, or inconsistently asserted that portions of the structure in Wu are different things depending upon the need for such structures to support the rejections.

Wu specifically states that the "SOI substrate 100 includes a silicon substrate 103, a buried oxide layer 102, and a P-type silicon layer 101." Col. 2, ll. 62-64; Figure 3. Wu further

states that "the SOI substrate 100 is a commercially available product formed by a SIMOX method…." Col. 2, ll. 65-67. Wu also states that "an oxygen ion implantation process 202 is then performed to form a silicon dioxide insulating layer 104 in the P-type silicon layer 101." Col. 3, ll. 7-9. Note that Wu does not state that the silicon dioxide layer 104 was formed in the silicon substrate 103. Wu goes on to note that "the silicon layer 101 **divides** into an upper and lower layer, which are denoted as the first silicon layer 101a and the second silicon layer 101b, respectively." Col. 2, ll. 13-15 (emphasis added). In the discussion regarding Figure 5 (which does appear to correspond to the disclosure), the substrate 100 is subjected to an oxygen implantation process 204 to form self-aligned oxygen-doped regions 212 in the second silicon layer 101b. Col. 3, l. 62 – Col. 4, l. 2. Thereafter, a heating process is performed to convert the oxygen-doped regions 212 into oxidation regions 212a. Wu also states that the second silicon layer 101b serves as a back gate electrode. Col. 3, ll. 15-16.

C. Claims 1-30 are Allowable Over the Prior Art of Record

Independent claims 1, 13 and 23 all recite that the multiple thickness buried oxide layer is formed between the bulk substrate and the active layer and that a substantially planar upper surface of the multiple thickness buried oxide layer contacts the active layer and the non-planar lower surface of the buried oxide layer contacts the bulk substrate. It is respectfully submitted that the Examiner erred in rejecting these independent claims, as well as all claims depending therefrom, in view of Wu, considered individually or in combination with any other art of record.

According to the Examiner, the SOI substrate in Wu comprises the buried oxide layer 102 (as specifically defined in Wu) and a multiple thickness buried oxide layer (the combination of the silicon dioxide layer 104 and the oxidation regions 212a). That is, the Examiner asserts that the SOI substrate is Wu comprises **two buried insulation layers**. Not only is this contrary

to the typical structure of SOI substrates, it is also contrary to the express teachings in Wu. Wu states that the SOI substrate 100 is comprised of the substrate 100, the buried oxide layer 102 and the layer of silicon 101. This is consistent with the understanding of such structures in the art and with the present disclosure wherein the SOI substrate is comprised of the bulk substrate 12, the buried oxide layer 20 and the active layer 21.

Wu does not anticipate nor render obvious the inventions defined in independent claims 1, 13 and 23 for a variety of reasons. Independent claims 1, 13 and 23 recite that the non-planar lower surface of the multiple thickness buried oxide layer contacts the bulk substrate. This is clearly not the case in Wu. In Wu, the lower surface of the combination of the oxide layer 104 and the oxide regions 212a is formed in the active layer to thereby divide the active layer into two layers 101a and 101b. See, *e.g.*, Figure 5. That is, the lower surface of the "multiple thickness buried oxide layer" identified by the Examiner does not contact the bulk substrate 103 shown in Wu. As noted by Wu, the lower surface of the "multiple thickness buried oxide layer" contacts the layer 101b, which serves as a back gate electrode. Col. 3, ll. 15-16. As clearly seen in Figures 7, 8 and 9, the oxidation regions 212a do not contact the bulk substrate 103 of the device disclosed in Wu. Thus, the Examiner erred in rejecting claims 1, 13 and 23 as being anticipated by Wu.

Moreover, the inventions defined by independent claims 1, 13 and 23, and all claims depending therefrom, cannot be considered as obvious in view of Wu, considered individually or in combination with any other art of record. There is certainly no suggestion in Wu that the oxidation regions 212a disclosed therein be positioned such that they contact the bulk substrate 103 disclosed in Wu. If anything, Wu can be said to teach away from such a configuration. There is simply no motivation suggested or disclosed in the art of record why one skilled in the

art would be motivated to form the oxidation regions 212a disclosed in Wu at a deeper depth than what is depicted therein.

Presumably, the device disclosed in Wu functions for its intended purpose. Thus, it is unclear why one skilled in the art would be motivated to position the oxidation regions 212a at a location other than that depicted in Wu, much less at the much deeper location so that the oxidation regions 212a would contact the bulk substrate 103. Even if Wu were combined with any other art of record, such a combination of prior would still not teach this limitation. Thus, any obviousness rejection based upon Wu would necessarily be legally improper. A recent Federal Circuit case makes it crystal clear that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. It is respectfully submitted that any attempt to assert that the inventions defined by the pending claims are obvious in view of the prior art of record constitutes an impermissible use of hindsight using Applicants' disclosure as a roadmap.

The Examiner's anticipation rejections of claims 1-30 should be REVERSED.

C. Claims 56-64 are Allowable Over the Prior Art of Record

Independent claims 56, 58 and 60 likewise recite that the buried oxide layer is formed between the bulk substrate and the active layer and that the substantially planar upper surface of the buried oxide layer contacts the active layer and the non-planar lower surface of the buried oxide layer contacts the bulk substrate as discussed above with respect to claims 1, 13 and 23. Thus, it is believed that independent claims 56, 58 and 60, and all claims depending therefrom,

are allowable over the art of record for at least the reasons set forth above with respect to independent claims 1, 13 and 23.

Additionally, independent claims 56, 58 and 60 further require the presence of a doped back gate region positioned at least partially in the bulk substrate under the buried oxide layer. It is believed that independent claims 56, 58 and 60 are allowable over the art of record for at least this additional reason. In Wu, it is clear that the active layer 101 is **divided** into a first silicon layer 101a and a second silicon layer 101b, wherein the second silicon layer 101b serves as a back gate electrode. Col. 3, ll. 13-16. However, it is also abundantly clear that the second silicon layer 101b is positioned above the layer 104 and is not formed at all in the bulk silicon layer 103. Thus, the device disclosed in Wu is in stark contrast to the device set forth in independent claims 56, 58 and 60. As before, there is no suggestion to modify the teachings of Wu so as to arrive at the inventions set forth herein. Again, it is not understood why one skilled in the art would be motivated to undertake efforts to form a back gate electrode at a deeper depth than what is depicted in Wu, particularly beyond the insulating layer 104 described therein, as set forth in independent claims 56, 58 and 60. For at least these additional reasons, it is believed that the Examiner erred in rejecting independent claims 56, 58 and 60, and all claims depending therefrom.

Accordingly, it is respectfully requested that the Examiner's rejection of claims 56-64 be REVERSED.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1-30 and 56-64 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

Applicants do not rely upon any evidence as indicated on the attached Evidence Appendix.

X. RELATED PROCEEDINGS APPENDIX

There are no Related Proceedings for this appeal as indicated on the attached Related Proceedings Appendix.

XI. CONCLUSION

Accordingly, it is respectfully submitted that the Examiner erred in not allowing claims 1-30 and 56-64 over the prior art of record. Applicants respectfully request the Board reverse the Examiner's rejections. The undersigned attorney may be contacted at (713) 934-4055 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

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CLAIMS APPENDIX

1. A semiconductor device, comprising:

a bulk substrate and an active layer;

a multiple thickness buried oxide layer formed between said bulk substrate and said active layer, said multiple thickness buried oxide layer having a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate; and

said active layer being formed above said multiple thickness buried oxide layer, said semiconductor device being formed in said active layer above said multiple thickness buried oxide layer.

2. The device of claim 1, wherein said bulk substrate is comprised of silicon.

3. The device of claim 1, wherein said semiconductor device is a transistor.

4. The device of claim 1, wherein said semiconductor device is part of at least one of a microprocessor, a memory device and a logic device.

5. The device of claim 1, wherein said active layer is comprised of silicon.

6. The device of claim 1, wherein said active layer has a thickness ranging from approximately 5-30 nm.

7. The device of claim 1, wherein said buried oxide layer is comprised of silicon dioxide.

8. The device of claim 1, wherein said multiple thickness buried oxide layer comprises:

a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections.

9. The device of claim 1, wherein said semiconductor device is a transistor having a channel region, at least a portion of said channel region being positioned above a section of said buried oxide layer that has a thickness that is less than a thickness of a remaining portion of said buried oxide layer.

10. The device of claim 1, wherein said semiconductor device is a transistor comprised of a gate electrode and wherein said multiple thickness buried oxide layer has a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than a thickness of said second sections, said first section being at least partially positioned under said gate electrode.

11. The device of claim 1, wherein said semiconductor device is a transistor comprised of a gate electrode and wherein said multiple thickness buried oxide layer has a first

section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than a thickness of said second sections, said first section being substantially aligned with said gate electrode.

12. The device of claim 8, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

13. A transistor, comprising:

a bulk substrate and an active layer;

a buried oxide layer formed between said bulk substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate, a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections; and

said active layer being formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer.

14. The transistor of claim 13, wherein said bulk substrate is comprised of silicon.

15. The transistor of claim 13, wherein said transistor is part of at least one of a microprocessor, a memory device and a logic device.

16. The transistor of claim 13, wherein said active layer is comprised of silicon.

17. The transistor of claim 13, wherein said active layer has a thickness ranging from approximately 5-30 nm.

18. The transistor of claim 13, wherein said buried oxide layer is comprised of silicon dioxide.

19. The transistor of claim 13, wherein said transistor comprises a channel region, at least a portion of said channel region being positioned above at least a portion of said first section of said buried oxide layer.

20. The transistor of claim 13, wherein said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is at least partially positioned under said gate electrode.

21. The transistor of claim 13, wherein said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is substantially aligned with said gate electrode.

22. The transistor of claim 13, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

23. A transistor comprised of a channel region, said transistor comprising:

a bulk silicon substrate and an active layer;

a buried oxide layer formed between said bulk silicon substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate, a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections; and

said active layer being formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer.

24. The transistor of claim 23, wherein said transistor is part of at least one of a microprocessor, a memory device and a logic device.

25. The transistor of claim 23, wherein said active layer is comprised of silicon.

26. The transistor of claim 23, wherein said active layer has a thickness ranging from approximately 5-30 nm.

27. The transistor of claim 23, wherein said buried oxide layer is comprised of silicon dioxide.

28. The transistor of claim 23, wherein said transistor further comprises a gate electrode and wherein said first section of said buried oxide layer is at least partially positioned under said gate electrode.

29. The transistor of claim 23, wherein said transistor further comprises a gate electrode and wherein said first section of said buried gate oxide layer is substantially aligned said gate electrode.

30. The transistor of claim 23, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

56. A semiconductor device, comprising:

a bulk substrate and an active layer;

a multiple thickness buried oxide layer formed between said bulk substrate and said active layer, said multiple thickness buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate;

said active layer being formed above said multiple thickness buried oxide layer, said semiconductor device being formed in said active layer above said multiple thickness buried oxide layer; and

a doped back gate region positioned at least partially in said bulk substrate under said multiple thickness buried oxide layer.

57. The device of claim 56, wherein said multiple thickness buried oxide layer comprises:

a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections.

58. A transistor, comprising:

a bulk substrate and an active layer;

a buried oxide layer formed between said bulk substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate, a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections;

said active layer formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer; and

a doped back gate region positioned at least partially in said bulk substrate under said buried oxide layer.

59. The transistor of claim 58, wherein said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is substantially aligned with said gate electrode.

60. A transistor comprised of a channel region, said transistor comprising:

a bulk silicon substrate and an active layer;

a buried oxide layer formed between said bulk silicon substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate, a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections;

said active layer formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer; and

a doped back gate region positioned at least partially in said bulk substrate under said buried oxide layer.

61. The transistor of claim 60, wherein said transistor further comprises a gate electrode and wherein said first section of said buried gate oxide layer is substantially aligned said gate electrode.

62. The device of claim 1, further comprising a doped back gate region positioned at least partially on said bulk substrate under said multiple thickness buried oxide layer.

63. The transistor of claim 13, further comprising a doped back gate region positioned at least partially on said bulk substrate under said buried oxide layer.

64. The transistor of claim 23, further comprising a doped back gate region positioned at least partially on said bulk substrate under said buried oxide layer.

EVIDENCE APPENDIX

Applicants do not rely on any evidence for this appeal.

RELATED PROCEEDINGS APPENDIX

There are no Related Proceedings for this appeal